Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended) An anti-fuse transistor formed on a semiconductor material comprising:

a polysilicon gate over a channel region in a substrate, the channel having a preset length;

a diffusion region proximate to a first end of the channel region;

~~an isolation~~ a field oxide region proximate to a second end of the channel region;

a variable thickness gate oxide between the polysilicon gate and the substrate, the variable thickness gate oxide having

a thick gate oxide portion extending from the first end of the channel region to a predetermined distance of the preset length,

a thin gate oxide portion extending from the predetermined distance to the second end of the channel region;

a breakdown resistant access edge proximate to the first end of the channel region for conducting current between the polysilicon gate and the diffusion region; and

an oxide breakdown zone proximate to the second end of the channel region, the oxide breakdown zone fusible to form a conductive link between the polysilicon gate and the channel region.

Claim 2 (Cancelled)

Claim 3 (Currently Amended) The anti-fuse transistor of claim 1, wherein the thin gate oxide portion ~~is identical~~ corresponds to ~~at least one low voltage transistor~~ a gate oxide of a low voltage transistor formed on the semiconductor material.

Claim 4 (Currently Amended) The anti-fuse transistor of claim 3, wherein the thick gate oxide portion ~~is identical~~ corresponds to ~~at least one high voltage transistor~~ another gate oxide of a high voltage transistor formed on the semiconductor material.

Claim 5 (Original) The anti-fuse transistor of claim 4, wherein the thick gate oxide portion includes a combination of an intermediate gate oxide and the thin gate oxide portion.

Claim 6 (Currently Amended) The anti-fuse transistor of claim 1 ~~2~~, wherein the floating diffusion region, the second end of the channel region and a gate edge of the polysilicon gate have a common edge defined by at least two line segments being at an angle to each other.

Claim 7 (Original) The anti-fuse transistor of claim 6, wherein the angle is one of 135 degrees and 90 degrees.

Claim 8 (Currently Amended) The anti-fuse transistor of claim 4, wherein the diffusion region has an LDD implant ~~identical~~ corresponding to ~~the~~ another LDD implant of one of the low voltage transistor, the high voltage transistor, and a combination of both the low and the high voltage transistors.

Claim 9 (Original) The anti-fuse transistor of claim 1, wherein an edge of the diffusion region and a portion of the polysilicon gate is free of salicidation.

Claim 10 (Original) An anti-fuse memory array comprising:

a plurality of anti-fuse transistors arranged in rows and columns, each anti-fuse transistor including

a polysilicon gate over a channel region in a substrate, the channel having a preset length;

a diffusion region proximate to a first end of the channel region;

a variable thickness gate oxide between the polysilicon gate and the substrate, the variable thickness gate oxide having a thick gate oxide portion extending from the first end of the channel region to a predetermined distance of the preset length, and a thin gate oxide portion extending from the predetermined distance to a second end of the channel region,

an oxide breakdown zone proximate to the second end of the channel region fusible to form a conductive link between the polysilicon gate and the channel region;

bitlines coupled to the diffusion regions of a column of anti-fuse transistors; and,

wordlines coupled to the polysilicon gates of a row of anti-fuse transistors.

Claim 11 (Original) The anti-fuse memory array of claim 10, further including a sense amplifier coupled to a pair of bitlines through isolation devices.

Claim 12 (Original) The anti-fuse memory array of claim 11, further including wordline decoding circuitry for selectively accessing one anti-fuse transistor coupled to one of the pair of bitlines for a single-ended sensing operation, and for selectively accessing another anti-fuse transistor coupled to the other of the pair of bitlines for a different address.

Claim 13 (Original) The anti-fuse memory array of claim 11, further including wordline decoding circuitry for selectively accessing one anti-fuse transistor coupled to one of the pair of bitlines and one anti-fuse transistor coupled to the other of the pair of bitlines for a dual-ended sensing operation.

Claim 14 (Currently Amended) The anti-fuse memory array of claim 10, further including column select pass gates coupled to the bitlines, at least one of the column select pass gates having a gate oxide ~~identical~~ corresponding to the thick gate oxide portion.

Claim 15 (Cancelled)
Claim 16 (Cancelled)
Claim 17 (Cancelled)
Claim 18 (Cancelled)

Claim 19 (Cancelled)
Claim 20 (Cancelled)
Claim 21 (Cancelled)
Claim 22 (Cancelled)

Claim 23 (Original) An anti-fuse transistor formed on a semiconductor material comprising:

an active channel area;

a polysilicon gate formed over the active channel area to define a fusible edge and an access edge;

a thick gate oxide adjacent to the access edge;

a first diffusion region adjacent to the access edge;

a second diffusion region adjacent to the fusible edge; and

a thin gate oxide over the active channel area adjacent to the fusible edge, the thin gate oxide having a lower breakdown voltage than the thick gate oxide for forming a conductive link between the polysilicon gate and the active channel area.

Claim 24 (Original) The anti-fuse transistor of claim 23, wherein a length of the fusible edge is defined by at least two line segments of the polysilicon gate being at an angle to each other.

Claim 25 (Currently Amended) The anti-fuse transistor of claim 23, wherein a length of the fusible edge is greater than a ~~width~~ length of the access edge ~~active channel area~~.

Claim 26 (Original) The anti-fuse transistor of claim 23, wherein the polysilicon gate defines the active channel area between the fusible edge and the access edge, and the thick gate oxide and the thin gate oxide are disposed between the channel region and the polysilicon gate, the thick gate oxide extending from the access edge to a predetermined length of the active channel area, and the thin gate oxide extending from the predetermined length of the active channel area to the fusible edge.

Claim 27 (Original) The anti-fuse transistor of claim 26, wherein the thick gate oxide is a combination of an intermediate oxide and the thin oxide.

Claim 28 (Original) The anti-fuse transistor of claim 26, wherein the polysilicon gate has

a first portion disposed over the thick gate oxide and located adjacent to the diffusion region for defining the active channel area, the access edge being defined by a first portion edge, and

a second portion disposed over the thin gate oxide and coupled to the first portion, the fusible edge being defined by a second portion edge, the second diffusion region being disposed between the fusible edge and the active channel area.

Claim 29 (Currently Amended) An anti-fuse transistor formed on a semiconductor material comprising:

an active channel area;

a polysilicon gate formed over the active channel area to define a fusible area~~,~~ and an access edge ~~and an isolation edge~~;

a thick gate oxide adjacent to the access edge;

a diffusion region adjacent to the access edge;

a field oxide adjacent to the fusible area ~~isolation edge~~; and

a thin gate oxide having ~~a~~ the fusible area between the thick gate oxide and the field oxide ~~isolation edge~~, the fusible area having a lower breakdown voltage than the thick gate oxide for forming a conductive link between the polysilicon gate and the active channel area.

Claim 30 (New) An anti-fuse transistor formed on a semiconductor material comprising:

a polysilicon gate over a channel region in a substrate, the channel having a preset length;

a diffusion region proximate to a first end of the channel region;

an isolation region proximate to a second end of the channel region;

a variable thickness gate oxide between the polysilicon gate and the substrate, the variable thickness gate oxide having

a thick gate oxide portion corresponding to a gate oxide of a high voltage transistor formed on the semiconductor material and extending from the first end of the channel region to a predetermined distance of the preset length,

a thin gate oxide portion corresponding to a gate oxide of a low voltage transistor formed on the semiconductor material and extending from the predetermined distance to the second end of the channel region;

a breakdown resistant access edge proximate to the first end of the channel region for conducting current between the polysilicon gate and the diffusion region; and

an oxide breakdown zone proximate to the second end of the channel region, the oxide breakdown zone fusible to form a conductive link between the polysilicon gate and the channel region.

Claim 31 (New) The anti-fuse transistor of claim 30 wherein the isolation region includes one of a field oxide region, a floating diffusion region and a combination of the field oxide and the floating diffusion regions proximate to the thin gate oxide portion.